# Advanced Analog Integrated Circuits

# Operational Transconductance Amplifier II
# Multi-Stage Designs

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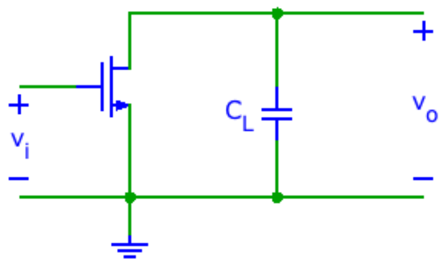
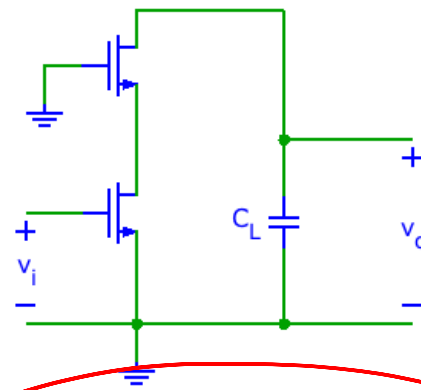
# Voltage Gain




- Low gain
- High swing

- High gain
- Red. swing

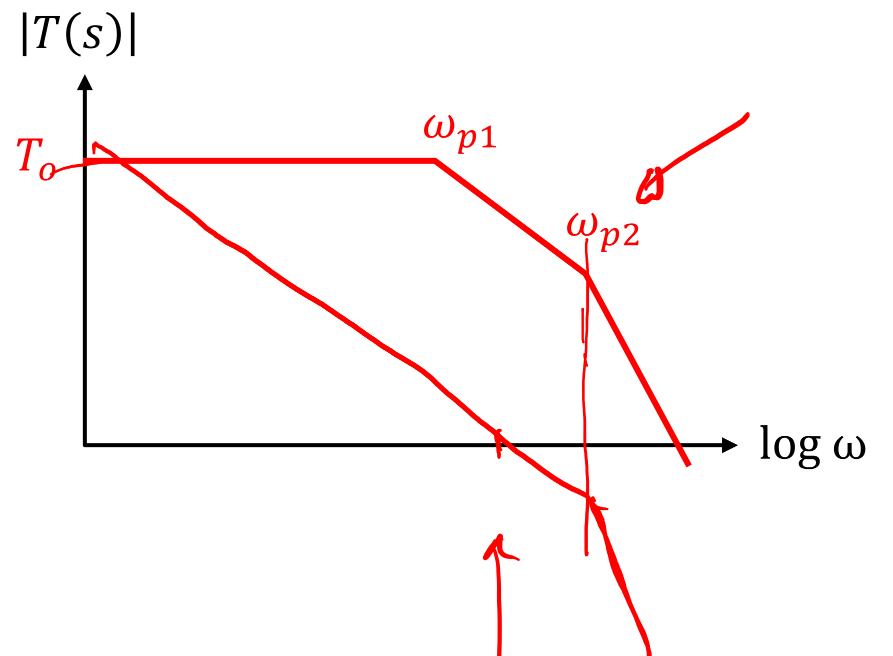
# Power Dissipation

| Voltage gain stage | Single Stage | Multiple Stage |
| --- | --- | --- |
| • Bias current | "single path to GND" | Multiple Bias currents |
| • Output swing | limited by cascodes | higher |

# Frequency Compensation

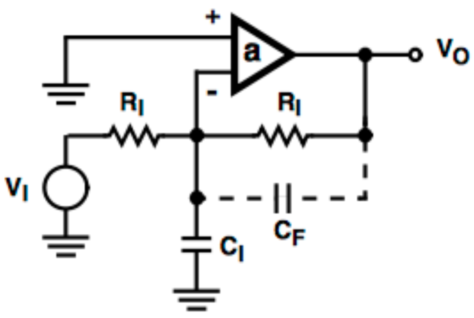
- Cascaded amplifiers
  - Each stage contributes a pole
  - Stability: only one "dominant pole" ($f_p < f_u$ of $T(s)$)
  - Ensuring this is called "compensation"
- Main compensation techniques
  - Narrowbanding
  - Feedback zero
  - Miller
  - Feedforward

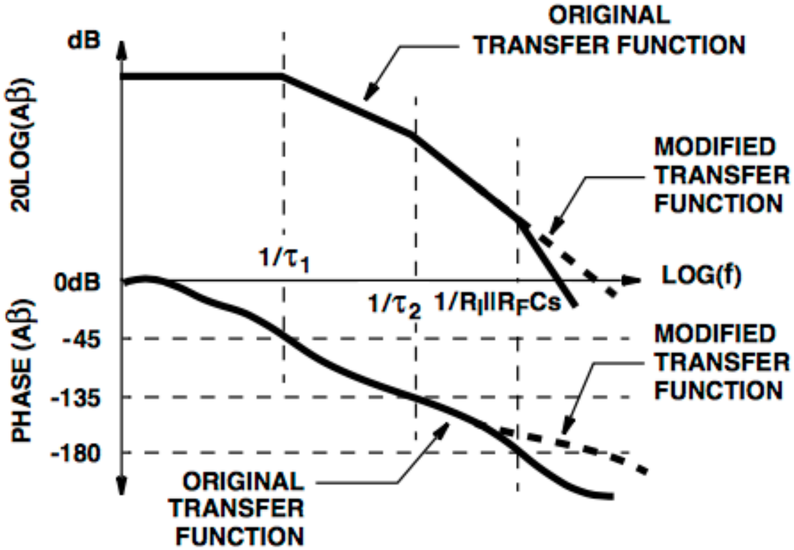
# Narrowbanding



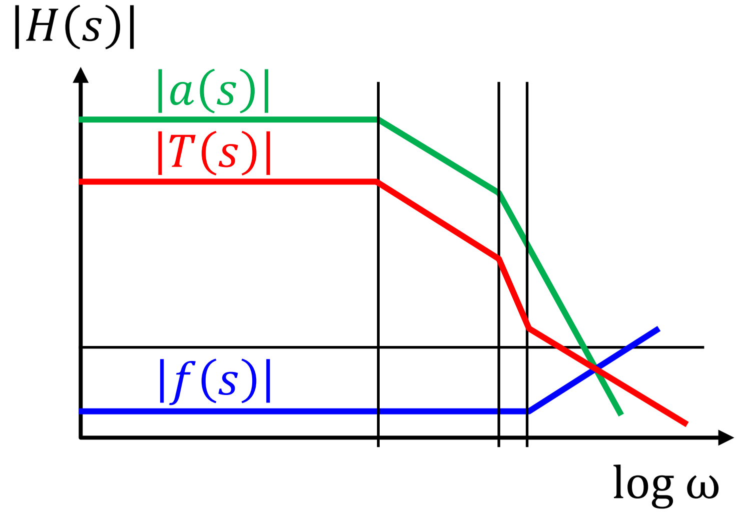

$$\omega_u \approx \frac{\omega_{p2}}{3}$$

# Feedback Zero



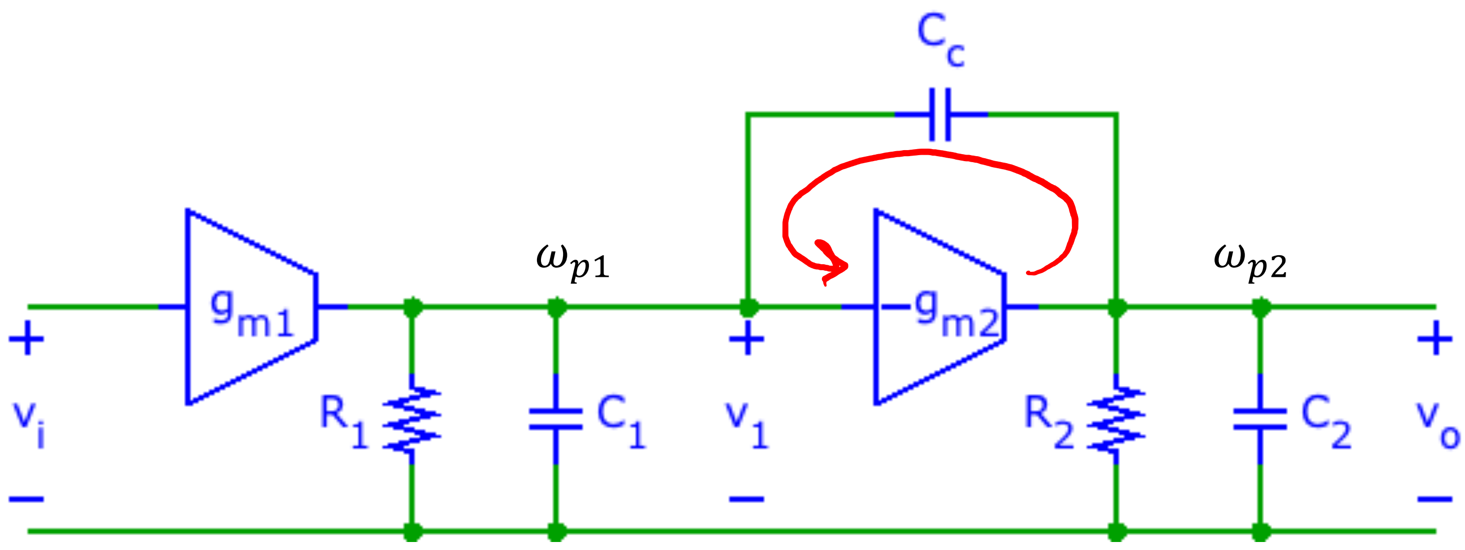




- LHP zero adds "lead"
- Closed-loop response modified above zero
- Compensation only marginally reduces bandwidth

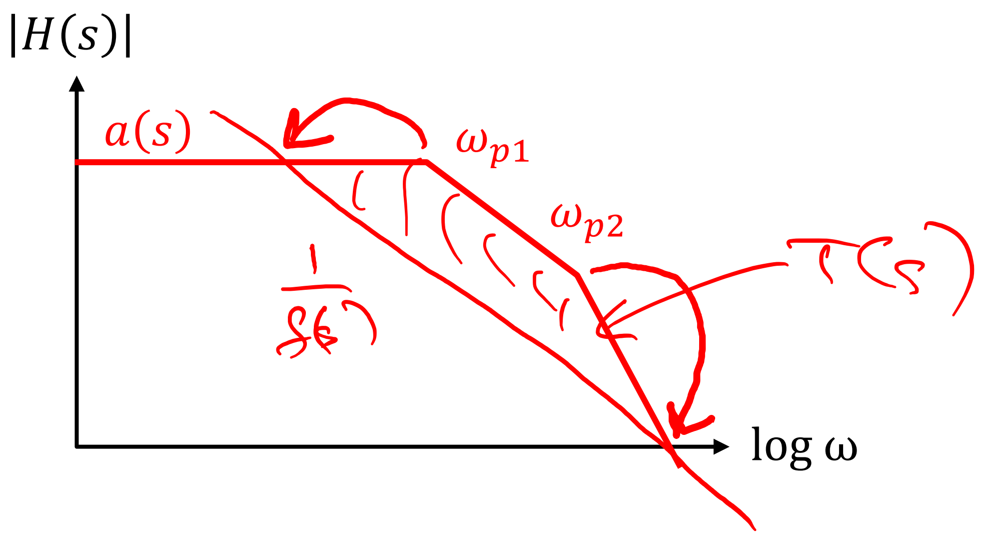



Ref: Feedback, Op Amps and Compensation, AN 9415.3, Intersil, Nov. 1996.

# Miller Compensation



# Intuitive Appreciation of Pole Splitting




- Capacitive feedback splits the poles

# Compensated *a(s)*

$$p_1 \cong -\frac{1}{R_1 \underbrace{g_{m2} R_2}_{\text{Miller gain}} C_c}$$

$$p_2 \cong -\frac{g_{m2}}{C_2\left(1+\frac{C_1}{C_c}\right)+C_1} \cong -\frac{g_{m2}}{C_2}$$

$$z = +\frac{g_{m2}}{C_c}$$

$$\text{GBW} = \omega_u \cong |\omega_{p1}| T_o = \beta \frac{g_{m1}}{C_c}$$

# Bandwidth Comparison

## Single voltage gain stage

$$\omega_u \cong \beta \frac{g_{m1}}{C_L}$$

$$\omega_{nd} \cong \frac{\omega_T}{3}$$

## Two voltage gain stages

$$\omega_u \cong \beta \frac{g_{m1}}{C_c}$$

$$\omega_{nd} = \omega_{p2} \cong \frac{g_{m2}}{C_L} = \underbrace{\frac{g_{m2}}{C_1}}_{\omega_{T2}} \underbrace{\frac{C_1}{C_L}}_{<1?}$$

$$\frac{\omega_{T2}}{3}$$

$C_L$ ↑ PM ↑

PM ↓

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# Miller Zero

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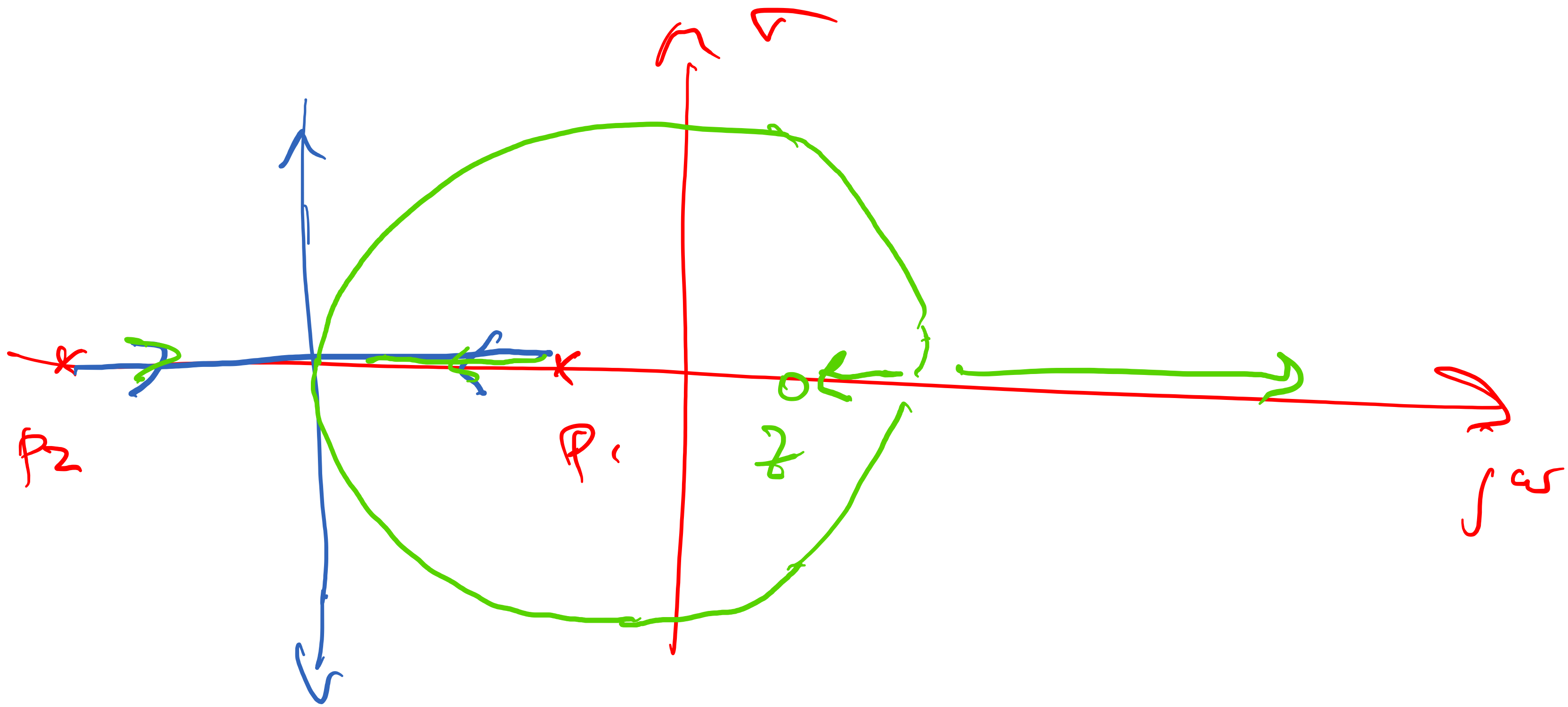
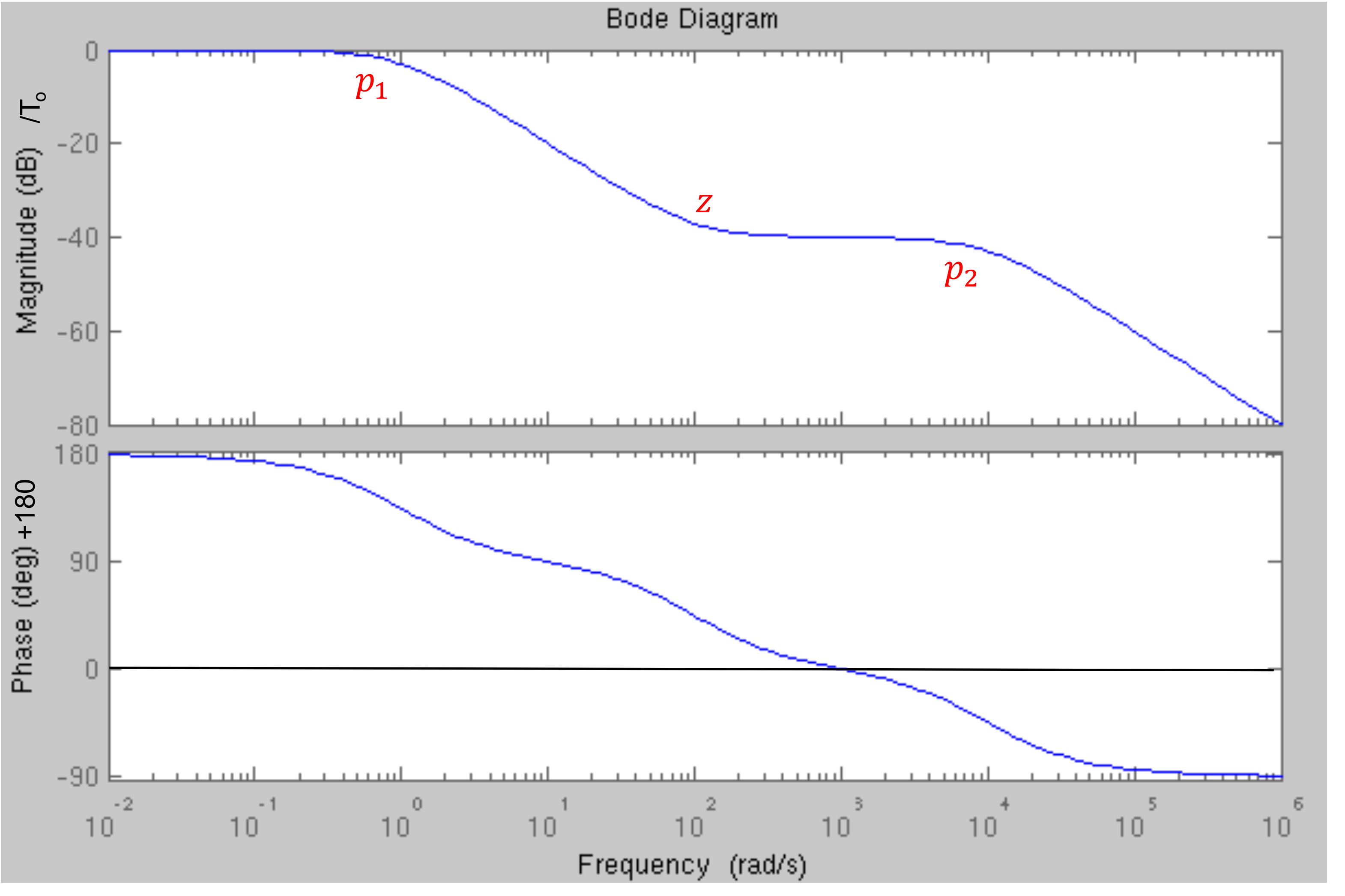
# Root Locus ← zero

**Ignoring zero** **With zero**

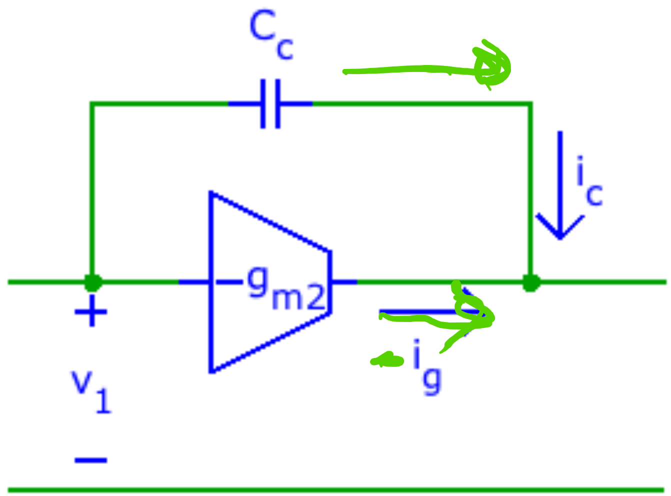


# Bode Plot



Bode Diagram
Magnitude (dB) /T_o
0
-20
-40
-60
-80
p_1
z
p_2
Phase (deg) +180
180
90
0
-90
10^-2
10^-1
10^0
10^1
10^2
10^3
10^4
10^5
10^6
Frequency (rad/s)

# Intuitive Appreciation of Zero



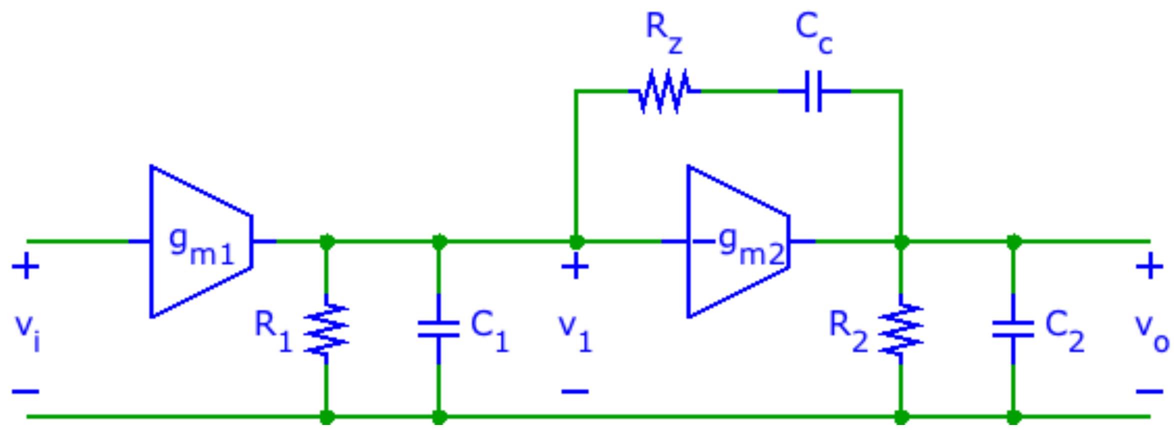
# Mitigating Impact of Zero

Key: unilateral feedback

Options:

- SF
- Ahuja comp
- Nulling resistor

# Nulling Resistor




$$T(s) = T_o \frac{1 - sC_c\left(\frac{1}{g_{m2}} - R_z\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)\left(1 - \frac{s}{p_3}\right)}$$

- $R_z$ can be used to "tune" the zero
- Poles $p_1$ and $p_2$ unchanged
- Additional pole $p_3 \cong -\frac{1}{R_z C_1}$

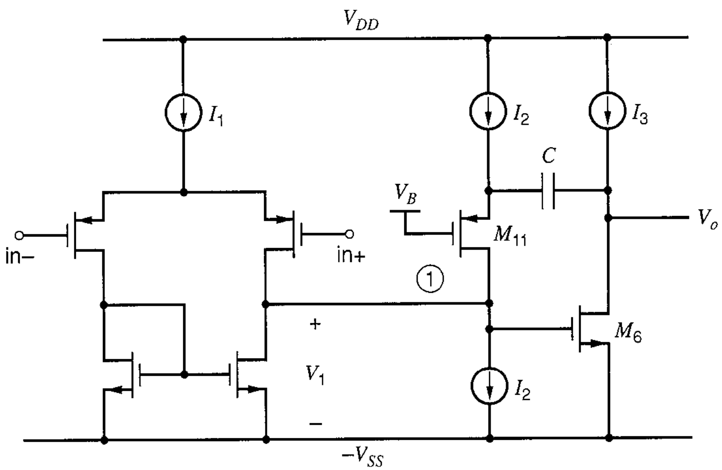
# Choices for $R_z$

~~a)~~ $R_z = 1/g_{m2}$

b) $R_z = \frac{1 + \frac{C_2}{C_c}}{g_{m2}}$ $\omega_{p3} \cong \frac{\omega_{T2}}{1 + \frac{C_2}{C_c}}$

cancel $p_2$

# Ahuja Compensation




[ Ahuja, IEEE JSSC, 12/1983 ]

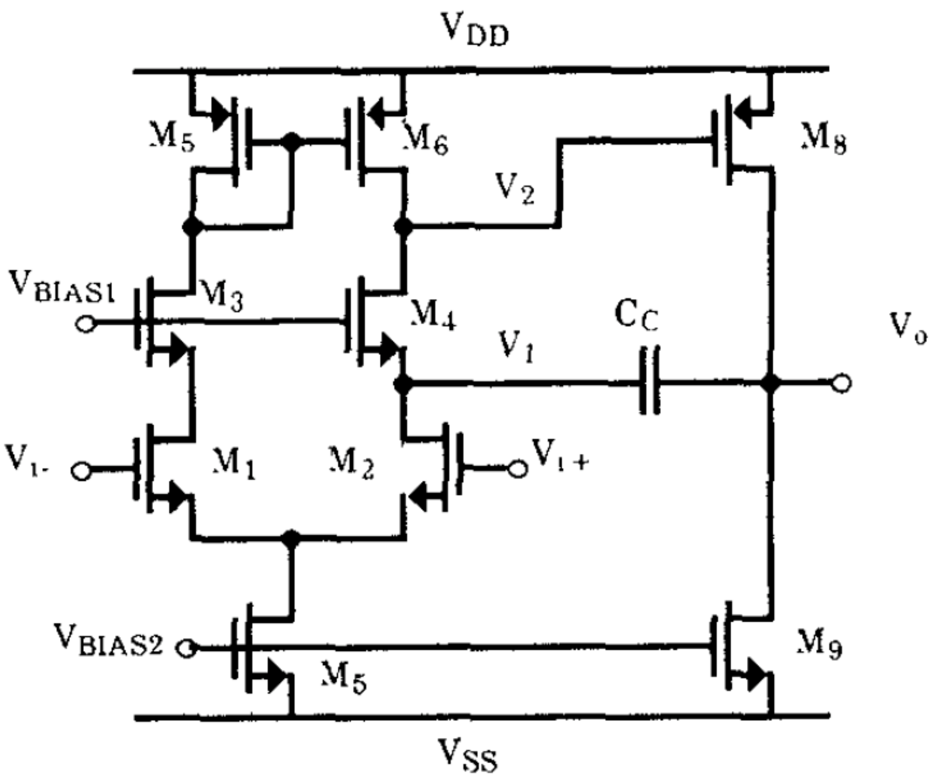
$$p_1 \approx -\frac{1}{(1+g_{m2}R_2)R_1C_c} \approx -\frac{g_{m1}}{a_{v0}C_c}$$

$$p_2 \approx -\frac{g_{m2}}{C_c + C_2}\frac{C_c}{C_1}$$

$$= p_2^* \underbrace{\frac{C_2}{C_c + C_2}\frac{C_c}{C_1}}_{\text{usually } >1}$$

- No zero (ideal cascode)
- $p_2$ at higher frequency
- Translates into smaller $C_c$ for given $C_2$
- Problems:
  - Current $I_2$ (extra power)
  - Mismatch (in $I_2$ sources) causes offset
  - $I_2$ limits slew rate

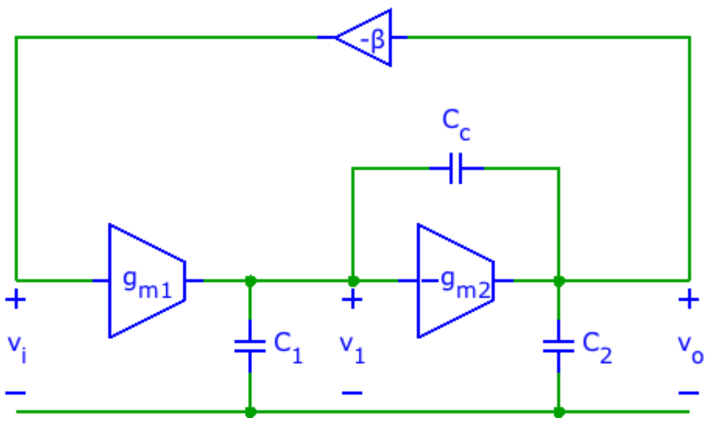
# Ribner Variant




- Uses 1st stage cascode to make feedback unilateral
- No extra power or slewing limitation
- 3rd order response
  - very challenging design problem

[ Ribner, IEEE JSSC, 12/1984 ]

# Noise Analysis




$$\overline{v_{oT}^2} = \frac{\gamma\alpha_1}{\beta}\cdot\frac{kT}{C_c}\left(1+\beta\frac{\alpha_2}{\alpha_1}\cdot\frac{C_c}{C_{Ltot}}\right)$$

- For full treatment, see

A. Dastgheib and B. Murmann, “Calculation of total integrated noise in analog circuits,” IEEE TCAS I, Nov. 2008, pp. 2988-93.

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# Design Example

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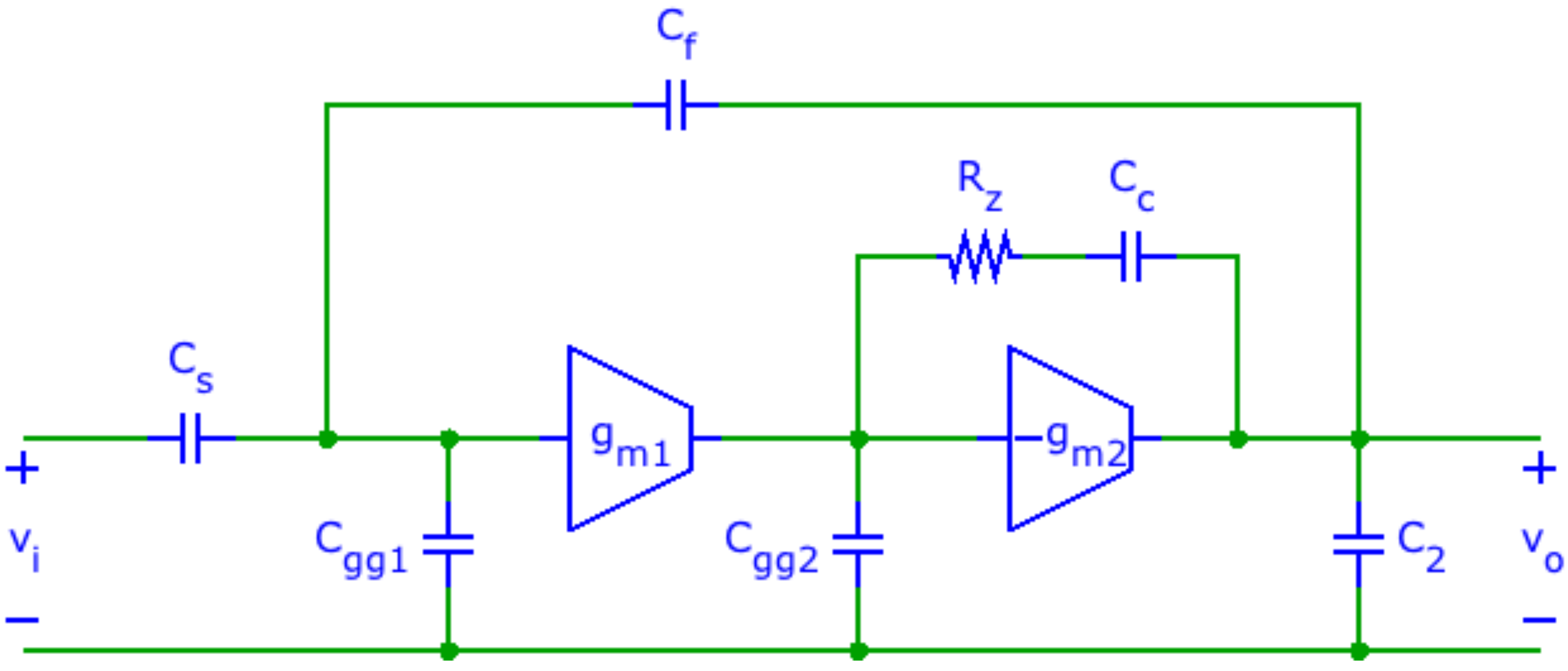

# Specification

| | | |
|---|---|---|
| Closed-loop gain (magnitude): | $A_{vo} := 2$ | |
| Settling time: | $t_s := 2ns$ | $f_{s\_max} := \frac{1}{2 \cdot t_s} = 250 \cdot MHz$ |
| Dynamic settling accuracy: | $\varepsilon_d := 0.02\%$ | |
| Dynamic range at output: | $DR := 10^{6.5}$ | $10 \cdot \log(DR) = 65$ dB |
| Sampling capacitance: | $C_s := 2pF$ | |
| Load capacitance: | $C_L := \frac{C_s}{A_{vo}} = 1\,pF$ | |
| Supply voltage: | $V_{dd} := 1.8V$ | |
| Zero mitigation: | $R_z = \frac{1}{g_{m2}}$ | |
| Power: | minimum | |

# Unknowns

- Topology
- Device parameters:
  - $M_1$: $g_{m1},\ V_1^*,\ f_{T1} \quad \Longrightarrow \quad I_{D1},\ L_1,\ W_1$
  - $M_2$: $g_{m2},\ V_2^*,\ f_{T2} \quad \Longrightarrow \quad I_{D2},\ L_2,\ W_2$
- Compensation capacitance, $C_c$
- Noise excess factors, $\alpha_1,\ \alpha_2$
- Output voltage range

# Structural Parameters

- Guess (and iterate):

| | | |
|---|---|---|
| M1 channel lenght: | $L_1 := 250\text{nm}$ | |
| M2 channel length: | $L_2 := 250\text{nm}$ | |
| Available output voltage range: | $V_{opp} := V_{dd} - 300\text{mV} = 1.5\,\text{V}$ | |
| OTA noise factor (topology & bias): | $\alpha_1 := 2$ | $\alpha_2 := 2$ |
| $C_{gg1}$ as a fraction of Cs+Cf: | $r_{gg1} := 1$ | |
| $C_{gg2}$ as a fraction of $C_{Ltot}$: | $r_{gg2} := 1$ | |

- Now calculate remaining design parameters …

# Gain and Feedback Factor

| | | |
|---|---|---|
| Feedback capacitance: | $C_f := \frac{C_s}{A_{vo}}$ | $C_f = 1 \cdot pF$ |
| M1 gate capacitance (guess): | $C_{gg1} := r_{gg1} \cdot (C_s + C_f)$ | $C_{gg1} = 3 \cdot pF$ |
| Feedback factor: | $\beta := \frac{C_f}{C_f + C_s + C_{gg1}}$ | $\beta = 0.167$ |
| Total load capacitance: | $C_{Ltot} := C_L + (1 - \beta) \cdot C_f$ | |

# Dynamic Range

Total noise at output: $N_{ot} := \dfrac{\frac{1}{2}\cdot\left(\frac{V_{opp}}{2}\right)^2}{DR}$ $\sqrt{N_{ot}} = 298.227 \cdot \mu V$

Compensation capacitance:

guess (for MathCad): $C_c := 1pF$

actual value: given $N_{ot} = \dfrac{\alpha_1}{\beta}\cdot\dfrac{k_B \cdot T_r}{C_c}\cdot\left(1 + \beta\cdot\dfrac{\alpha_2}{\alpha_1}\cdot\dfrac{C_c}{C_{Ltot}}\right)$ $\text{find}(C_c) = 0.568\,pF$

# Settling

Settling time (single pole, no slewing): $t_s = -0.7 \cdot \tau \cdot \ln(\varepsilon_d)$

Settling time constant: $\tau := \dfrac{-t_s}{0.7 \cdot \ln(\varepsilon_d)} = 335.456 \cdot \text{ps}$

Settling time constant: $\tau = \dfrac{C_c}{\beta \cdot g_{m1}}$ $\qquad \omega_u := \dfrac{1}{\tau} = 474.444 \cdot \text{MHz} \cdot 2\pi$

Transconductance of M1: $g_{m1} := \dfrac{C_c}{\beta \cdot \tau} = 17.886 \cdot \text{mS}$

Nondominant pole (~73 deg PM): $\omega_{p2} := 3.3 \cdot \omega_u = 1.566\,\text{GHz} \cdot 2\pi$

Gate capacitance of M2 (guess): $C_{gg2} := r_{gg2} \cdot C_{Ltot} = 1.833\,\text{pF}$

Transconductance of M2: $g_{m2} := \omega_{p2} \cdot \left[C_{Ltot} \cdot \left(1 + \dfrac{C_{gg2}}{C_c}\right) + C_{gg2}\right] = 69.135\,\text{mS}$

# Power Dissipation

Cutoff frequency of M1: $\omega_{T1} := \frac{g_{m1}}{C_{gg1}} = 0.949\,\text{GHz} \cdot 2\pi$

Cutoff frequency of M2: $\omega_{T2} := \frac{g_{m2}}{C_{gg2}} = 6.002\,\text{GHz} \cdot 2\pi$

M1 power efficiency (lookup): $V_{1star} := 85\text{mV}$ ←

Close to weak inversion:

- increase $L_1$ (higher gain)
- reduce $r_{gg1}$ (lower power?)

M2 power efficiency (lookup): $V_{2star} := 120\text{mV}$

M1 drain current: $I_{d1} := 0.5 \cdot V_{1star} \cdot g_{m1} = 760.159\,\mu\text{A}$

M2 drain current: $I_{d2} := 0.5 \cdot V_{2star} \cdot g_{m2} = 4.148\,\text{mA}$

Power dissipation: $P_t := V_{dd} \cdot (I_{d1} + I_{d2}) = 8.835\,\text{mW}$

# Iteration: $r_{gg1} = 0.1$

| | |
|---|---|
| Cutoff frequency of M1: | $\omega_{T1} := \frac{g_{m1}}{C_{gg1}} = 5.219\,\text{GHz} \cdot 2\pi$ |
| Cutoff frequency of M2: | $\omega_{T2} := \frac{g_{m2}}{C_{gg2}} = 5.788\,\text{GHz} \cdot 2\pi$ |
| M1 power efficiency (lookup): | $V_{1star} := 120\text{mV}$ |
| M2 power efficiency (lookup): | $V_{2star} := 120\text{mV}$ |
| M1 drain current: | $I_{d1} := 0.5 \cdot V_{1star} \cdot g_{m1} = 590.241\,\mu\text{A}$ |
| M2 drain current: | $I_{d2} := 0.5 \cdot V_{2star} \cdot g_{m2} = 3.703\,\text{mA}$ |
| Power dissipation: | $P_t := V_{dd} \cdot (I_{d1} + I_{d2}) = 7.728\,\text{mW}$ |

was 8.8 mW

# Sanity Check: Single Gain Stage

$$\tau_1 := \frac{-0.7 \cdot t_s}{\ln(\varepsilon_d)} = 164.373\,\text{ps}$$

$$g_m := \frac{C_{Ltot}}{\beta \cdot \tau_1} = 34.069\,\text{mS}$$

$$C_{gg} := 0.5 \cdot (C_s + C_f) = 1.5\,\text{pF} \qquad \omega_T := \frac{g_m}{C_{gg}} = 3.615\,\text{GHz} \cdot 2\pi \qquad V_{star} := 100\text{mV}$$

$$I_d := 0.5 \cdot g_m \cdot V_{star} = 1.703\,\text{mA} \qquad P_1 := V_{dd} \cdot I_d = 3.066\,\text{mW}$$

- About half the power of 2-stage
  - Provided gain & dynamic range can be met
  - Practical “lower bound”

# Finalize Design

- Iterate over all parameters (use Matlab “lookup”)
- Estimate and add extrinsic capacitances
- Other design elements
  – Static settling error
  – Slewing
  – Biasing
  – Device geometry
  – Corners
  – Layout …

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# Special OTA Topologies

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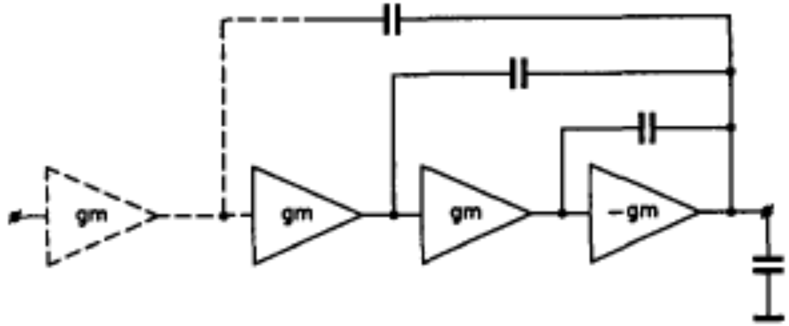
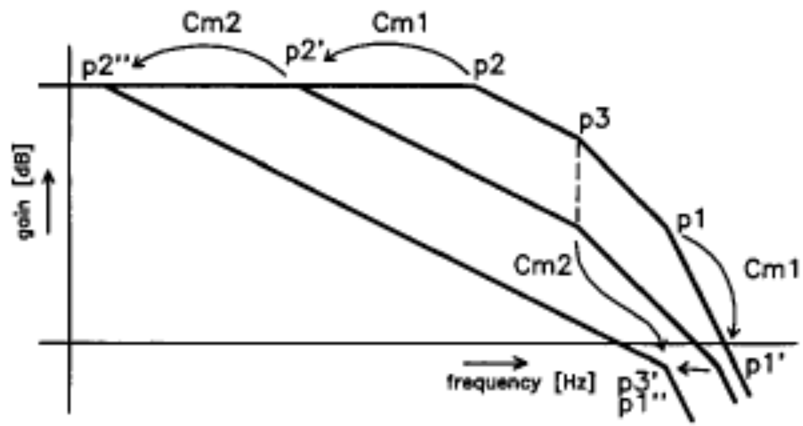
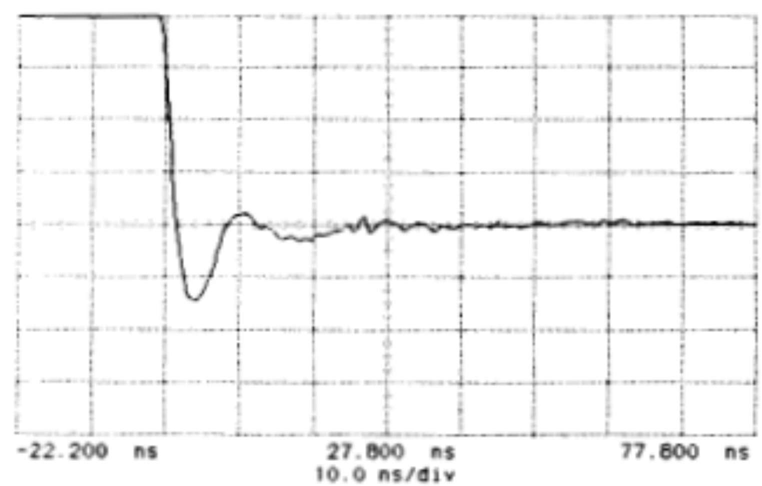
# Nested Miller Compensation



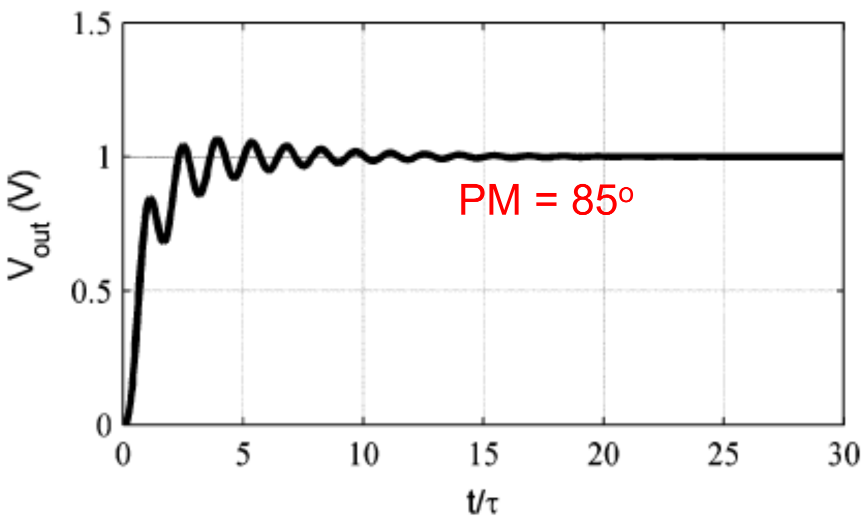




Ref: R. Eschauzier et al, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure", IEEE JSSC, Dec. 1992, pp. 1709-1717.

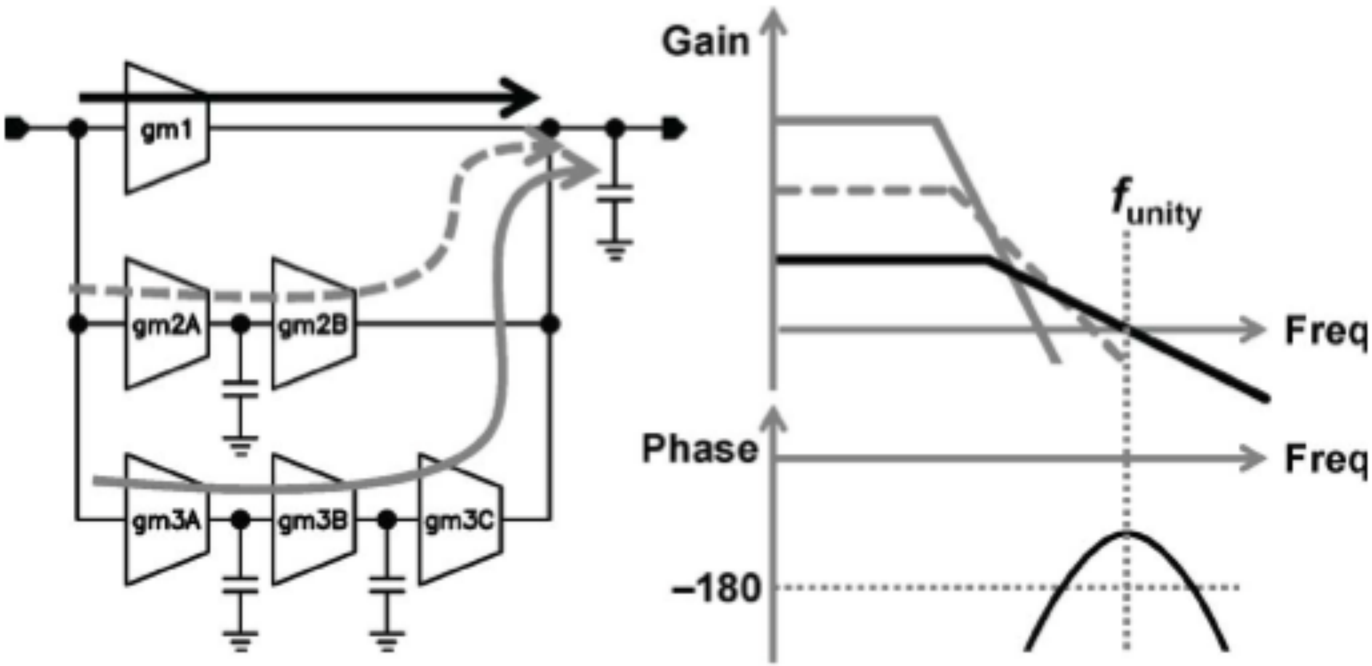
# Settling Behavior

- Very challenging design problem
- Accurate and fast settling (nearly?) impossible
- Good choice for broad-band, high gain & other situations that do not require fast settling




Ref: Nguyen & Murmann, "The Design of Fast-Settling Three-Stage Amplifiers Using the Open-Loop Damping Factor as a Design Parameter", IEEE TCAS I, June 2010, pp. 1244-54.

# Feedforward OTA




Ref: Shibata et al, "A DC-to-1 GHz Tunable RF ΔΣ ADC Achieving DR=74dB and BW=150MHz at $f_o$=450MHz Using 550 mW", JSSC 12/2012, pp. 2888-97.